What is claimed is:

1. A method for exposing chip patterns on a wafer, the method comprising:

providing a photomask which includes a first mask pattern and a second mask pattern, the first mask pattern having first chip patterns and arranged in an area corresponding to a maximum exposure area of a projection exposure apparatus, and the second mask pattern having second chip patterns different from the first chip patterns and arranged adjacently to the first mask pattern;

aligning the maximum exposure area of the projection exposure apparatus with a part of the first mask pattern and a part of the second mask pattern;

exposing a part of the first chip patterns and a part of the second chip patterns on a first wafer;

aligning the maximum exposure area of the projection exposure apparatus with the first mask pattern; and

exposing the first chip patterns on a second wafer.

2. The method according to Claim 1, wherein the first mask pattern is a mask pattern for mass-production.

3. The method according to Claim 1, wherein the first mask pattern is provided at the center of the photo mask and the second mask pattern is provided at the periphery of the first mask pattern.

4. A method for exposing chip patterns on a wafer, the method comprising:

providing a photomask which includes a main mask pattern and a sub-mask pattern, the main mask pattern having a first size corresponding to a maximum exposure area of a projection exposure apparatus and having first chip patterns, and the sub-mask pattern having a second size smaller than the first size and having second chip patterns different from the first chip patterns and provided adjacently to the main mask pattern;

aligning the maximum exposure area of the projection exposure apparatus with an area of the first size comprised of a part of the main mask pattern and a part of the sub-mask pattern;

exposing a part of the first chip patterns and a part of the second chip patterns in the area of the first size on a first wafer;

aligning the maximum exposure area of the projection exposure apparatus with an area of the first size of the main mask pattern; and

exposing the first chip patterns in the area of the first size on a second wafer.

5. The method according to Claim 4, wherein the main mask pattern is a mask pattern for mass-production.

6. The method according to Claim 4, wherein the main mask pattern is set at the center of the photo mask and the sub-mask pattern is set at the periphery of the main mask pattern.

7. A photomask comprising:

a first mask pattern which has first chip patterns and which has a first size corresponding to a maximum exposure area of a projection exposure apparatus; and

a second mask pattern which has second chip patterns different from the first chip patterns, which has a second size smaller than the first size, and which is arranged adjacently to the first mask pattern.

8. The photomask according to Claim 7, wherein the first mask pattern is a mask pattern for mass-production.

9. The photomask according to Claim 7, wherein the first mask pattern is provided at the center of the photo mask and the second mask pattern is provided at the periphery of the first mask pattern.

10. A photomask comprising:

a main mask pattern having first chip patterns and having a first size corresponding to a maximum exposure area of a projection exposure apparatus; and

a sub-mask pattern having second chip patterns different from the first chip patterns, having a second size smaller than the first size, and arranged adjacently to the main mask pattern.

11. The photomask according to Claim 10, wherein the main mask pattern is a mask pattern for mass-production.

12. The photomask according to Claim 10, wherein the main mask pattern is provided at the center of the photo mask and the sub-mask pattern is provided at the periphery of the main mask pattern.